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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PHAM, HAI CHI	
ART UNIT	**PAPER NUMBER**
2861	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/873,256	EMA ET AL.	
	Examiner	Art Unit	
	Hai C. Pham	2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-26* is/are allowed.

6)☒ Claim(s) *27-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 08/05/05. These drawings are accepted.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 27, 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Kanai (JP 11-10949).

Kanai discloses a multi-beam image forming apparatus comprising a plurality of light-emitting parts (laser unit 2 having at least two light-emitting parts LD1 and LD2) each configured to output a light flux, an optical scanning unit (polygon mirror 5), which scans the plurality of light fluxes on a medium to be scanned (photoconductor 7), the light fluxes being synchronous with an output pixel clock and being modulated in accordance with image data of a respective one of a plurality of lines (the start of modulation of each of the light-emitting parts LD1 and LD2 for each scanning line is in synchronization with the synchronous detection signal DETP1), and a clock phase control circuit which controls a phase of said output pixel clock for each of said lines (the clock processing IC 14 producing the pixel clocks VCLK1 and [delayed] VCLK2 by synchronizing the output

pixel clocks in phase with the synchronous detection signal DETP1 using the phase synchronous circuits 23a-23b) so as to correct a shift in a write start position in a scanning direction due to a shift in a position of each light-emitting point of said plurality of light fluxes (see Problem To Be Solved section of the Abstract).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 28 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanai in view of Ogasawara et al. (U.S. 6,154,246).

Kanai discloses all the basic limitations of the claimed invention including a high-frequency clock (VCLK), the first frequency divider (24b), but except for the phase change circuit for changing the phase of the first frequency divider and the second frequency divider, which generates an internal clock by dividing the high-frequency clock.

Ogasawara et al. discloses an image forming apparatus comprising a high-frequency clock generation circuit (crystal oscillating circuit 31), a first frequency divider (half frequency dividing circuit 35), which generates and outputs an image clock (image processing clock PCLK), which synchronized with an output of a photodetector (BD signal) by dividing a clock output from the high-frequency clock generation circuit, and

an image clock phase control circuit (BD synchronization circuit 65), which changes a phase of the image clock for each of the scanning lines so as to correct a shift in a write start position in the main scanning direction (col. 7, lines 59-65). Ogasawara et al. further teaches the clock phase control circuit comprising a phase change circuit for changing the phase of the first frequency divider (the first frequency divider 35 starts the frequency division in synchronism with the timing determined by the rising edge of the synchronous detection signal), and a second frequency divider (quarter frequency dividing circuit 36), which generates an internal clock by dividing an output of said high-frequency clock generator, the second frequency divider having a circuit, which can change a phase of said internal clock. Ogasawara et al. also teaches a modulation pattern generation circuit (38), which generates a modulation pattern (image modulating signal PVDO) based on said image data and the clock output from said high-frequency clock generation circuit, a semiconductor laser control circuit (laser drive circuit 81), which controls the output of said semiconductor laser based on the modulation pattern generated by the modulation pattern generation circuit, wherein the first frequency divider, the image clock phase change circuit, the high-frequency clock generating circuit, the image data input circuit and the modulation pattern generation circuit are constituted by an integrated circuit formed in a single semiconductor chip (IC 11) (Fig. 1).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide the phase change circuit and the second frequency divider in the device of Kanai as taught by Ogasawara et al. The motivation for

doing so would have been to further suppress any phase error between the image processing clock and the synchronous detection signal as suggested by Ogasawara et al. at col. 7, lines 21-30.

6. Claims 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanai in view of Ogasawara et al., as applied to claims 27-28 above, and further in view of Ishida et al. (U.S. 6,498,617).

Kanai, as modified by Ogasawara et al., discloses all the basic limitations of the claimed invention including said high-frequency clock generation circuit having a PLL circuit (39) comprising a voltage controlled oscillator (VCO 32), which controls an oscillation frequency of a clock, a phase comparator circuit (33) and wherein said first frequency divider (35) generates said output pixel clock by dividing an output of said voltage controlled oscillator circuit and a phase of said output pixel clock is synchronized with the phase synchronous signal (e.g., in synchronism with the rising edge of the synchronous detection signal), but except for the programmable counter.

Ishida et al. discloses an image forming apparatus including a clock generator having a PLL circuit having a programmable divider (59) (Fig. 16), which is also a frequency dividing ratio, which can be arbitrarily set/change by a user (col. 21, lines 51-65).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the programmable frequency divider in the

modified device of Kanai as taught by Ishida et al. The motivation for doing so would have been to accurately lock the phase of the reference clock generating circuit.

7. Claims 36 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanai in view of Swanberg (U.S. 4,694,156).

Kanai discloses all the basic limitations of the claimed invention except for the clock phase control circuit controlling a phase of said output pixel clock to correct a fluctuation in a scanning length.

Swanberg discloses an image forming apparatus comprising a pixel placement control for correcting a fluctuation in the scanning length corresponding to each of the facet of the polygon mirror wherein the phase control corrects a phase lag or a phase change according with the spot velocity and the pixel clock frequency (col. 7, lines 8-31).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the correction of the phase lag or advance in the device of Kanai as taught by Swanberg. The motivation for doing so would have been to ensure that every scanning line in a page has the same length.

8. Claims 37 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanai in view of Swanberg, as applied to claims 36 and 43 above, and further in view of Ogasawara et al.

Kanai, as modified by Swanberg, discloses all the basic limitations of the claimed invention except for the phase change circuit for changing the phase of the first frequency divider and the second frequency divider, which generates an internal clock by dividing the high-frequency clock.

Ogasawara et al. discloses an image forming apparatus comprising a high-frequency clock generation circuit (crystal oscillating circuit 31), a first frequency divider (half frequency dividing circuit 35), which generates and outputs an image clock (image processing clock PCLK), which synchronized with an output of a photodetector (BD signal) by dividing a clock output from the high-frequency clock generation circuit, and an image clock phase control circuit (BD synchronization circuit 65), which changes a phase of the image clock for each of the scanning lines so as to correct a shift in a write start position in the main scanning direction (col. 7, lines 59-65). Ogasawara et al. further teaches the clock phase control circuit comprising a phase change circuit for changing the phase of the first frequency divider (the first frequency divider 35 starts the frequency division in synchronism with the timing determined by the rising edge of the synchronous detection signal), and a second frequency divider (quarter frequency dividing circuit 36), which generates an internal clock by dividing an output of said high-frequency clock generator, the second frequency divider having a circuit, which can change a phase of said internal clock. Ogasawara et al. also teaches a modulation pattern generation circuit (38), which generates a modulation pattern (image modulating signal PVDO) based on said image data and the clock output from said high-frequency clock generation circuit, a semiconductor laser control circuit (laser drive circuit 81),

which controls the output of said semiconductor laser based on the modulation pattern generated by the modulation pattern generation circuit, wherein the first frequency divider, the image clock phase change circuit, the high-frequency clock generating circuit, the image data input circuit and the modulation pattern generation circuit are constituted by an integrated circuit formed in a single semiconductor chip (IC 11) (Fig. 1).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide the phase change circuit and the second frequency divider in the modified device of Kanai as taught by Ogasawara et al. The motivation for doing so would have been to further suppress any phase error between the image processing clock and the synchronous detection signal as suggested by Ogasawara et al. at col. 7, lines 21-30.

9. Claims 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanai in view of Swanberg and Ogasawara et al., as applied to claims 36-37 above, and further in view of Ishida et al.

Kanai, as modified, discloses all the basic limitations of the claimed invention except for the programmable counter.

Ishida et al. discloses an image forming apparatus including a clock generator having a PLL circuit having a programmable divider (59) (Fig. 16), which is also a frequency dividing ratio, which can be arbitrarily set/change by a user (col. 21, lines 51-65).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the frequency dividing ratio setting circuit or programmable frequency divider in the modified device of Kanai as taught by Ishida et al. The motivation for doing so would have been to accurately lock the phase of the reference clock generating circuit.

Allowable Subject Matter

10. Claims 1-26 are allowed.

11. The following is an examiner's statement of reasons for allowance: claims 1, 9, 14 and 22 are patentable over the prior art patents and printed publications because of the specific phase clock control circuit for use in an image forming apparatus, which includes a high-frequency clock generating circuit, a generator for generating load data and a phase set signal, a first frequency divider, which outputs an image clock in synchronism with an output of the photodetector by dividing the high-frequency clock by a frequency dividing number selected based on the load data, and an image clock phase changing circuit, which changes the phase of the image clock based on the phase set signal. The combined limitations as claimed are not taught by the prior art of record considered alone or in combination.

Claims 2-8, 10-13, 15-21 and 23-26 are allowable because they are directly or indirectly dependent from the above-mentioned claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

12. Applicant's arguments with respect to claims 27-44 have been considered but are moot in view of the new grounds of rejection as presented in this Office action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai C. Pham whose telephone number is (571) 272-2260. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (571) 272-1934. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hai C. Pham

HAI PHAM
PRIMARY EXAMINER
October 13, 2005

OBLON, SPIVAK, ET AL.
Docket No. 209412US2
Inventor: HIDETOSHI EMA, ET AL.
Serial No. 09/873,256
Reply to OA dated: May 11, 2005
Replacement Sheet

Approved
HEB
10/12/05

FIG.30